Embedded Systems

1. **Course number and name:** 020SEMES3 Embedded Systems

2. **Credits and contact hours:** 4 ECTS credits, 2x1:15 contact hours

3. **Name(s) of instructor(s) or course coordinator(s):** Jean Sawma

4. **Instructional materials:** Course handouts; lab experiments; slides; in-class problems

5. **Specific course information**
   a. **Catalog description:**
   Embedded systems: Introduction, motivation and applications – Types of the embedded systems – Integration and implementation levels – Variable types – Fixed and floating point variable formats – Schematics and PCBs – FGPA: Introduction, Basic Logic Element (BLE) architecture, input/output – Introduction to Quartus Prime and Altera FPGA – VHDL: Introduction, basics, combinatorial and sequential behavior, process and clocks, advanced concepts – Introduction to co-design: link between the hardware and the software – NIOS II processor creation and programming.

   b. **Prerequisites:** (020TEDNI4 Digital Systems Design or 020TEDCI4 Digital Systems Design) and (020IF1NI2 Programming 1 or 020IF1CI2 Programming 1)

   c. **Selected Elective** for CCE and EE students

6. **Educational objectives for the course**
   a. **Specific outcomes of instruction:**
   - Analyze the basic concepts of an embedded systems.
   - Understand fixed and floating point formats.
   - Understanding schematics and PCBs.
   - Develop a VHDL code for embedded system applications.
   - Understand and manipulate the software/hardware co-design concept.
   - Implement a complete co-design system inside an FPGA.

   b. **PI addressed by the course:**

PI	1.1	1.2	1.3	6.1	6.2	6.3	6.4	7.1
Covered	x	x	x	x	x	x	x	x
Assessed				x	x	x	x	

7. **Topics and approximate lecture hours**
   - Introduction to embedded systems, motivation and applications (2 lectures)
   - Fixed and floating point variables (2 lecture)

- Introduction to Quartus Prime, Modelsim and Altera FPGAs (2 lectures)
- Introduction to Schematics and PCBs (1 lectures)
- FPGA: Introduction, architecture of BLE, Programmable I/O and clocks (1 lectures)
- VHDL: Introduction, basics, concurrent and sequential instructions, combinatorial, structural and sequential behaviors, clocked process, advanced concepts (6 lectures)
- Hardware and software co-design (4 lecture)
- Lab sessions: Implementation of a clock divider and register in VHDL, implementation of an equation inside an FPGA in fixed point format, implementation of a stop watch in VHDL, control of a system using a hardware and software co-design, creation of a VGA using an FPGA (5 labs of 2:30 hours each)