Computer Architecture

1. **Course number and name:** 020AROES3 Computer Architecture

2. **Credits and contact hours:** 4 ECTS credits, 2x1:15 contact hours

3. **Instructor's or course coordinator's name:** Nathalie Matta

4. **Text book:**
   William Stallings, *Computer Organization and Architecture: Designing for Performance*, 9th edition, Prentice Hall, 2013
   a. **Other supplemental materials:**
      Instructor's handouts

5. **Specific course information**
   a. **Catalog description:**
      Computer evolution and performance - Von Neumann model – interconnection structures – memory systems - inputs / outputs - instruction sets – processor structure and function - pipelines - RISC and CISC – ILP and superscalar processors - parallel architectures and organizations

   b. **Prerequisites or co-requisites:** 020TEDNI4 Digital Systems Design or 020TEDCI4 Digital Systems Design

   c. **Required/Elective/Selected Elective:** Elective for CCE students; required for CCE software engineering option students

6. **Specific goals for the course**
   a. **Specific outcomes of instruction:**
      - Explain and describe the principles of computer architecture and organization
      - Understand, describe and evaluate the evolution of and advances in computer systems
      - Understand the various components of computer systems and their interaction
      - Demonstrate understanding of interrupt mechanisms, bus interconnections, and various bus interfaces
      - Describe different I/O mechanisms and peripherals
      - Understand and implement the memory hierarchy of a computer system (including registers, cache, internal memory, external storage)
      - Understand and compare various instruction set architectures of microprocessors, as well as instruction formats and addressing modes
      - Understand and apply pipelining concepts and control implementations in scalar and superscalar microprocessors
      - Describe and compare the parallel architectures and their implementations available on the market and understand the organization of these architectures

b. KPI addressed by the course:

KPI	a2	e1	h1	i2	j1
Covered	x	x	x	x	x
Assessed	x	x			x
Give Feedback					

7. Brief list of topics to be covered and approximate lecture hours

- Introduction, Computer Architecture / Organization, Computer Structure and Function, Computer History (1 lecture)
- Computer Evolution and Performance (1 lecture)
- Components and Interconnections: Instruction Cycle, Interrupts, Interconnection Structures, Buses, QPI (2 lectures)
- Computer Memory System Overview and Cache Memory: Characteristics, Performance, Organization, Memory Hierarchy, Locality of Reference, Cache Design and Organization, Examples (2 lectures)
- Exercises and problems (2 lectures)
- Internal Memory (Semiconductor Technologies, Organization, Packaging, Error Correction, and Advanced DRAM Organizations) (2 lectures)
- External Memory (Magnetic Disks, SSD, etc.) (1 lecture)
- Input/Output (External Devices, I/O Modules, Programmed and Interrupt- Driven I/O, Direct Memory Access, I/O Channels and Processors, Examples and exercises) (2 lectures)
- Exercises and problems (1 lecture)
- Instruction Sets: characteristics and functions, Instruction Formats and Addressing Modes (2 lectures)
- Processor structure and function: processor and register organization, instruction pipelining (2 lectures)
- Exercises and problems (2 lectures)
- Reduced instruction set computers: Reduced Instruction Set Architecture, RISC v/s CISC, RISC pipelining (2 lectures)
- Instruction-level parallelism and superscalar processors: Instruction-Level Parallelism and Machine Parallelism, Instruction Issue Policy, Register Renaming, Machine Parallelism, Branch Prediction, Superscalar Execution, Superscalar Implementation (2 lectures)
- Exercises and problems (2 lectures)
- Parallel organization: parallel processing, multicore computers (2 lectures)